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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/532,468 | 04/22/2005 | Harumitsu Miyashita | YAMAP0976US | 1625 |

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| EXAMINER | |
|---|---|
| GHULAMALI, QUTBUDDIN | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2611 | |

| MAIL DATE | DELIVERY MODE |
|---|---|
| 04/02/2008 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/532,468 | MIYASHITA ET AL. | |
| | Examiner | Art Unit | |
| | Qutbuddin Ghulamali | 2611 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *22 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13-20* is/are allowed.

6)☒ Claim(s) *1,12, 21-26* is/are rejected.

7)☒ Claim(s) *2-11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/22/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Specification*

1. The abstract of the disclosure is objected to because the abstract of the disclosure does not commence on a separate sheet in accordance with 37 CFR 1.52(b)(4). A new abstract of the disclosure is required and must be presented on a separate sheet, apart from any other text. Correction is required. See MPEP § 608.01(b).

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 12, 21-26 rejected under 35 U.S.C. 102 (b) as being anticipated by Reed et al (USP 6,023,386).

Regarding claims 1, 22-24, 26, Reed discloses a frequency and phase control apparatus, comprising:

a signal input section (20) for receiving a reproduction signal (col. 7, lines 45-55);

an analog/digital conversion section (sampling device 24) for converting the reproduction signal (62) into a multiple bit digital signal based on a clock signal (col. 7, lines 50-67; col. 8, lines 1-5);

a maximum likelihood decoding section for converting the multiple bit digital signal into a binary signal (col. 8, lines 11-17);

a pattern detection section (discrete time sequence detector) for detecting a pattern (sequence) of the binary signal (col. 8, lines 11-15);

a determination section for determining whether or not the multiple bit digital signal and the clock signal are in synchronization with each other based on the detection result (col. 2, lines 47-58; col. 8, lines 17-22; col. 9, lines 25-35; col. 10, lines 1-5); and a clock generation section for adjusting at least one of a frequency and a phase of the clock signal based on the detection result and outputting the adjusted clock signal (col. 7, lines 34-45), wherein when the determination result of the determination section indicates that the multiple bit digital signal and the clock signal are in synchronization with each other, the maximum likelihood decoding section generates a binary signal based on a first state transition rule (col. 11, lines 5-10, 19-36); and when the determination result of the determination section indicates that the multiple bit digital signal and the clock signal are not in synchronization with each other, the maximum likelihood decoding section generates a binary signal based on a second state transition rule (col. 5, lines 6-31; col. 11, lines 28-50).

Regarding claim 12, Reed discloses wherein when the determination result of the determination section (intervals) indicates that the multiple bit digital signal and the clock signal are in synchronization with each other, the maximum likelihood decoding section generates a binary signal based on a first state transition rule (col. 11, lines 5-10, 19-36); and when the determination result (i.e., plurality of synchronization

sequence) of the determination section indicates that the multiple bit digital signal and the clock signal are not in synchronization with each other, the maximum likelihood decoding section generates a binary signal based on a second state transition rule (col. 5, lines 6-31; col. 11, lines 28-50).

Regarding claim 21, Reed discloses a maximum likelihood decoder for receiving a multiple bit digital signal generated based on a clock signal (col. 8, lines 11-17) and a flag (sync mark) indicating whether or not the multiple bit digital signal and the clock signal are in synchronization with each other, and converting the multiple bit digital signal into a binary signal based on the flag (col. 2, lines 47-58; col. 8, lines 17-22; col. 9, lines 25-35; col. 10, lines 1-5; col. 11, lines 51-65), wherein:
when the flag indicates that the multiple bit digital signal and the clock signal are in synchronization with each other, the maximum likelihood decoder generates a binary signal based on a first state transition rule (col. 11, lines 5-10, 19-36), and when the flag indicates that the multiple bit digital signal and the clock signal are not in synchronization with each other, the maximum likelihood decoder generates a binary signal based on a second state transition rule (col. 5, lines 6-31; col. 11, lines 28-50).

Regarding claim 25, Reed discloses a method for reproducing information comprising:
a signal input section (20) for inputting a reproduction signal (col. 7, lines 45-55);
an analog/digital conversion section (sampling device 24) for converting the reproduction signal (62) into a multiple bit digital signal based on a clock signal (col. 7, lines 50-67; col. 8, lines 1-5);

a maximum likelihood decoding section for converting the multiple bit digital signal into a binary signal (col. 8, lines 11-17);

a pattern detection section (discrete time sequence detector) for detecting a pattern (sequence) of the binary signal (col. 8, lines 11-15);

a determination section for determining whether or not the multiple bit digital signal and the clock signal are in synchronization with each other based on the detection result (col. 2, lines 47-58; col. 8, lines 17-22; col. 9, lines 25-35; col. 10, lines 1-5);

a clock generation section for adjusting at least one of a frequency and a phase of the clock signal based on the detection result and outputting the adjusted clock signal (col. 7, lines 34-45); and

a reproduction section (read/write functions) for reproducing information from the information recording medium based on the adjusted clock signal (col. 7, lines 18-38.

***Allowable Subject Matter***

4. Claim 13-20 allowed.

5. Claims 2-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Conclusion***

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patents:

US Patent (6,003,153) to Shimoda.

US Patent (4,475,234) to Nishijima et al.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Qutbuddin Ghulamali whose telephone number is (571)-272-3014. The examiner can normally be reached on Monday-Friday, 7:00AM - 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

QG
March 25, 2008.

/CHIEH M FAN/
Supervisory Patent Examiner, Art Unit 2611